Evolution of Wafer Shape and Localized Stress of Silicon Surrounded by Through Silicon Via Patterns along Various Process Integration Steps

Chang Hwan Lee[1], Seok Ho Jie[1], Sang Hoon Son[1], Jong Tae Kim[1], Hyung Won Yoo[1], Il Keoun Han[1] and Woo Sik Yoo[2]

[1]Hynix Semiconductor Inc., San 136-1 Ami-ri Bubal-eub, Icheon, Gyeonggi, 446-701, Korea
[2]WaferMasters, Inc., 246 East Gish Road, San Jose, CA 95112, U.S.A.
Phone: +82-31-639-1465 E-mail: changhwan.lee@hynix.com

1. Introduction

Demands for high performance and highly functional devices are constantly increasing. Device scaling by miniaturization is becoming extremely difficult as it approaches physical limits of Si. As an alternative approach to traditional device scaling, three dimensional (3D) packaging using through silicon vias (TSVs) is being actively investigated. TSVs are typically filled with copper (Cu) to reduce resistance of interconnects. The development of stress, during various TSV fabrication steps, poses a risk of compromised device performance, reliability and yield loss [1-4].

In this paper, we have studied the evolution of wafer shape and localized stress of Si with TSV structures along various process integration steps.

2. Experiment

300mm diameter Si wafers with various TSV diameters and layouts are prepared with various fabrication steps. Figure 1 shows TSV fabrication process flow with wafer surface profile and Raman stress characterization steps. The effect of process steps on changes in wafer profile and Si stress is investigated.

Wafer shape was characterized using a very high resolution optical surface profiler (WaferMasters OSP-300) designed for blanket and device wafers [5]. Lattice level Si stress measurement and stress mapping was done using a fully automated, high resolution polychromator-based, multi-wavelength Raman spectroscopy system (WaferMasters MRS-300) [6].

Microscopic Raman spectroscopy is a very powerful, non-destructive characterization technique for crystallinity and stress/strain of semiconductor materials with sub-micrometer spatial resolution [7]. Intensity, shift, and full width at half maximum (FWHM) of Raman signals are measured to gain valuable information on important physical characteristics of the materials [6,7]. Multiwavelength excitation capability provides virtual depth profiling ability [6,7]. Three major spectral lines (457.9, 488.0 and 514.5nm) from a multi-wavelength Ar^+ ion laser are used as the excitation light source. Figure 2 shows a Raman spectroscopy scan method.

3. Results and Discussions

Figure 3 shows the evolution of wafer surface profile with five TSV fabrication steps, characterized using the OSP-300 system. Vector plots of surface normal, height contour map and wafer curvature along major crystal axes are summarized. The wafer surface profile goes through significant curvature changes as do bow-height characteristics, along process steps. Cu filling processes induced the most significant changes in curvature and bow height. Significant localized distortions were also noticed in all wafers.

Figure 4 shows Raman line scan results across three TSV structures, under 488.0nm excitation. The 56 point Raman line scan was done over 110µm, in 2µm intervals. Prior to TSV etch, the wafer appeared almost stress free, with Raman peak at ~520.3cm^{-1} regardless of excitation wavelength. Line scan results of Raman intensity were also plotted. The wafer with blanket Cu film, after Cu fill, did not show any Raman signal due to the total reflection of excitation laser beam. The shift of the Raman peak position towards the higher wavenumber side is proportional to the amount of compressive stress in Si ($\sigma_{xx} + \sigma_{yy} = -434.5\ \Delta\omega$ MPa) [7].

Raman shift variations up to ±0.5cm^{-1} (equivalent to stress variations of ±218MPa) were measured near the TSV structures. For the wafer with Cu-filled TSVs, Raman intensity was significantly lower on top of the TSVs and the Si next to the Cu-filled TSVs was compressively stressed.

We have confirmed that the wafer shape and localized stress of Si, surrounded by TSV structures, goes through significant changes along TSV fabrication process steps using wafer surface profiling and Raman spectroscopy. Significant increase of lattice level stress is expected in Si surrounded by high density, small diameter Cu-filled TSVs and may cause device performance variations and reliability issues. A large difference in thermal expansion coefficient between Si and Cu and Cu grain growth during subsequent annealing processes can induce significant stress and cause device reliability, performance variation and/or yield loss.

4. Summary

Wafer surface profiling and Raman stress characterization with stress simulation can enhance our understanding of the impact of TSV dimensions, layouts and process steps on Si stress and stress-induced device reliability problems.

References

[1] K.H. Lu et al, Proc. 59th Electronic Components and Technology Conf., San Diego, CA, 2009, 630.
[2] A. Trigg et al, Appl. Phys. Exp. 3 (2010) 086601.
[3] A. Trigg et al, Ext. Absts. Int. Conf. on Solid State Devices and Materials (2010) P-2-3.
[4] J. Gambino et al, ECS Trans., 35(4) (2011) 687.
[5] W.S. Yoo et al, ECS Trans., 35(4) (2011) 861.
[6] W.S. Yoo et al, Appl. Phys. Exp. 2 (2009) 116502.
[7] I. De Wolf, Semicond. Sci. Technol. 11, (1996) 139.

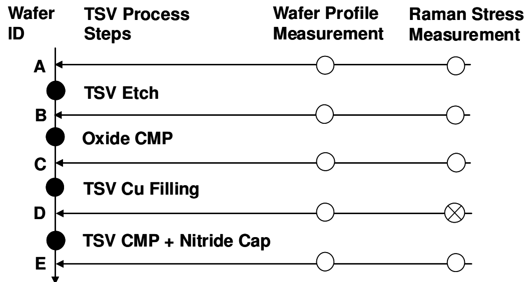

Fig. 1. TSV fabrication process flow and wafer surface profile and Raman stress characterization steps.

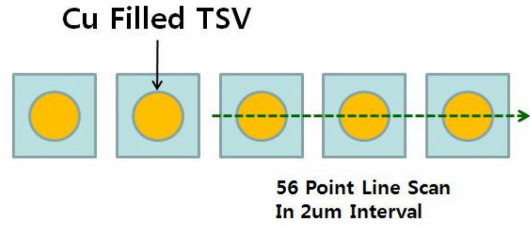

Fig. 2. Raman spectroscopy line scan location and interval.

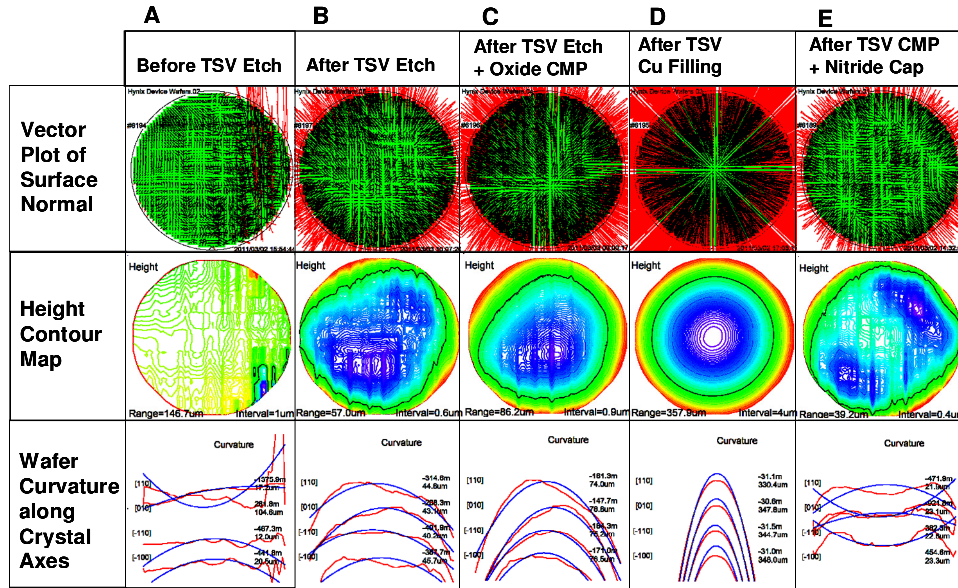

Fig. 3. Evolution of surface profile of 300mm Si wafers with TSV structures along Cu filled TSV integration steps.

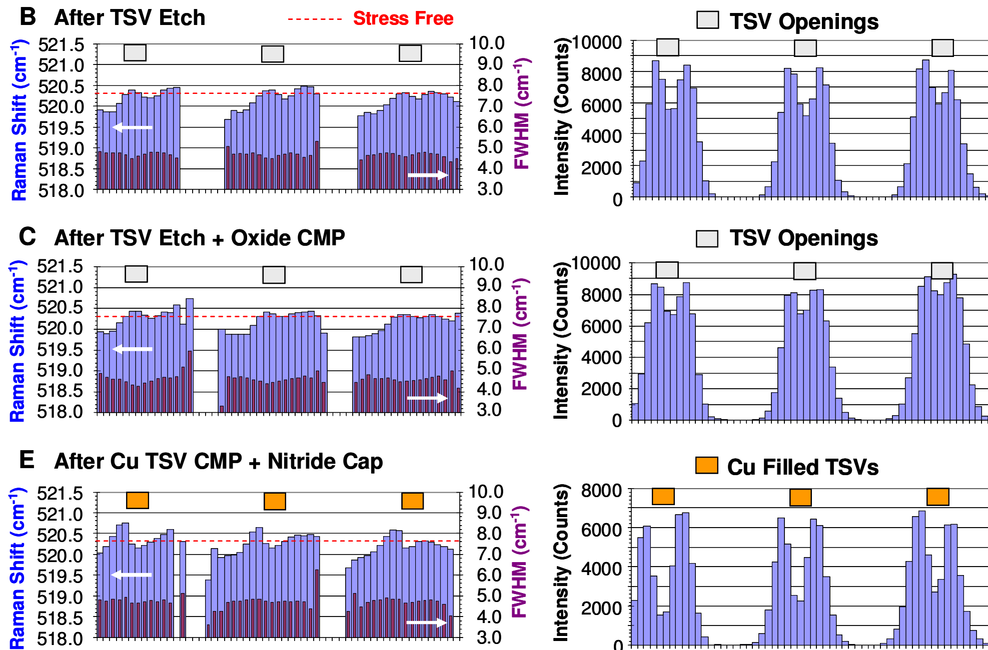

Fig. 4. Line scan summary of Raman shift, FWHM and intensity of Si region between 10μm diameter TSVs along process steps.